1. A method of preventing copper diffusion in the fabrication of an integrated circuit by means of a composite diffusion barrier layer comprising:

providing a substrate or wafer having an insulator layer deposited upon said substrate;

providing a first level of conducting wiring over said insulator layer;

depositing a first and second dielectric layer over said first level of conducting wiring;

patterning and etching the dielectric layers forming dual damascene trench/via openings;

depositing a WN first barrier layer over said dielectric layers covering and lining said trench/via;

soaking said WN first barrier layer in a reactive silane gas mixture to form a WSiN layer on the WN, thus forming a composite barrier layer consisting of top layer to bottom layer of WSiN/WN diffusion barrier layer.

2. The method of claim 1, wherein the substrate or wafer is semiconductor single crystal silicon or an IC module, with MOSFET or CMOS devices therein.

3. The method of claim 1, wherein both first and second dielectric layers are selected from the group

consisting of low dielectric materials, silicon dioxide and silicon oxide.

4. The method of claim 1, wherein the first barrier layer of WN is deposited by metal-organic chemical vapor deposition (MOCVD) from the reduction of tungsten organic precursors, or deposited by plasma-enhanced chemical vapor deposition (PECVD), or by physical vapor deposition (PVD), reactive sputtering, in the thickness range from about 60 to 400 Angstroms.

5. The method of claim 1, wherein the top barrier layer of W, when applicable, is deposited by chemical vapor deposition (CVD) or by physical vapor deposition (PVD), sputtering, in the thickness range from about 30 to 50 Angstroms.

6. The method of claim 1, wherein the trench or channel and via hole contact is lined with a diffusion barrier layer comprised of a composite barrier with a top layer of WSiN, thickness from about 30 to 60 Angstroms and a bottom layer of WN, thickness from about 30 to 50 Angstroms.

7. The method of claim 1, wherein the trench or channel and via hole contact is lined with a diffusion

barrier layer comprised of a composite barrier with top layer of W thickness from about 30 to 50 Angstroms, interposed or intervening layer of WSiN thickness from about 30 to 60 Angstroms, and bottom layer of WN thickness from about 60 to 400 Angstroms.

8. The method of claim 1, wherein the WN barrier layer is treated by an in situ soak process, whereby, a reactant silane gas mixture of either silane and ammonia, or silane and hydrogen, at between about 300 to 400 °C, forms a WSiN compound layer from about 30 to 60 Angstroms thick on the surface of the WN barrier layer.

9. The method of claim 1, wherein in the trench or channel and the via hole contact is lined with an adhesive copper seed layer on the diffusion barrier layer, the copper seed layer being deposited by electrochemical deposition (ECD), or by physical vapor deposition (PVD) sputtering, and the seed layer material is comprised of copper metal layer, thickness from about 1,000 to 2,200 Angstroms by PVD, and thickness from about 200 to 500 Angstroms by chemical vapor deposition (CVD).

10. The method of claim 1, wherein the conducting material layers for conducting interconnect lines and

via contacts comprise the following conducting type materials: electrochemical deposition (ECD) of copper, upon the copper seed layer.

11. The method of claim 1, wherein the ECD copper is electrochemically deposited in the trench/via structures with a wide process window upon said seed layer and said barrier layer, with a fine grained <111> texture.

12. The method of claim 1, wherein each level of conducting structure is planarized by removing excess material, the method being selected from the group consisting of: planarization by chemical mechanical polish (CMP), milling, ion milling, and/or etching, which leave the copper in trench/via openings, forming single and dual inlaid structures that include conducting interconnect lines and contact vias.

13. The method of claim 1, wherein multilevel conducting structures are fabricating by repeating the process described herein.

14. A method of preventing copper diffusion in the fabrication of an integrated circuit by means of a composite diffusion barrier layer comprising:

providing a substrate or wafer having an insulator layer deposited upon said substrate;

providing a first level of conducting wiring over said insulator layer;

depositing a first and second dielectric layer over said first level of conducting wiring;

patterning and etching the dielectric layers forming dual damascene trench/via openings;

depositing a WN first barrier layer over said dielectric layers covering and lining said trench/via;

soaking said WN first barrier layer in a reactive silane gas mixture forming a WSiN layer on the WN;

depositing a W barrier layer over said WN first barrier layer and over said WSiN layer, forming a composite barrier layer consisting of top layer to bottom layer of W/WSiN/WN diffusion barrier layer;

depositing by electrochemical deposition (ECD) a copper seed layer over said diffusion barrier layer;

depositing by electrochemical deposition (ECD) copper conducting material over said copper seed layer and removing the excess material layers to from conducting copper dual inlaid structures.

15. The method of claim 14, wherein the substrate or wafer is semiconductor single crystal silicon or an IC module, with MOSFET or CMOS devices therein.

16. The method of claim 14, wherein both first and second dielectric layers are selected from the group consisting of low dielectric materials, silicon dioxide and silicon oxide.

17. The method of claim 14, wherein the first barrier layer of WN is deposited by metal-organic chemical vapor deposition (MOCVD) from the reduction of tungsten organic precursors, or deposited by plasma-enhanced chemical vapor deposition (PECVD), or by physical vapor deposition (PVD), reactive sputtering, in the thickness range from about 60 to 400 Angstroms.

18. The method of claim 14, wherein the top barrier layer of W is deposited by chemical vapor deposition (CVD) or by physical vapor deposition (PVD), sputtering, in the thickness range from about 30 to 50 Angstroms.

19. The method of claim 14, wherein the trench or channel and via hole contact is lined with a diffusion barrier layer comprised of a composite barrier with top

layer of WSiN thickness from about 30 to 60 Angstroms, and bottom layer of WN thickness from about 60 to 400 Angstroms.

20. The method of claim 14, wherein the trench or channel and via hole contact is lined with a diffusion barrier layer comprised of a composite barrier with top layer of W thickness from about 30 to 50 Angstroms, interposed or intervening layer of WSiN thickness from about 30 to 60 Angstroms, and bottom layer of WN thickness from about 60 to 400 Angstroms.

21. The method of claim 14, wherein the WN barrier layer is treated by an in situ soak process, whereby, a reactant silane gas mixture of either silane and ammonia, or silane and hydrogen, at between about 300 to 400 °C, forms a WSiN compound layer from about 30 to 60 Angstroms thick on the surface of the WN barrier layer.

22. The method of claim 14, wherein in the trench or channel and the via hole contact is lined with an adhesive copper seed layer on the diffusion barrier layer, the copper seed layer being deposited by electrochemical deposition (ECD), or by physical vapor deposition (PVD) sputtering, and the seed layer material is comprised of copper metal layer, thickness from about

1,000 to 2,200 Angstroms by PVD, and thickness from about 200 to 500 Angstroms by chemical vapor deposition (CVD).

23. The method of claim 14, wherein the conducting material layers for conducting interconnect lines and via contacts comprise the following conducting type materials: electrochemical deposition (ECD) of copper, upon the copper seed layer.

24. The method of claim 14, wherein the ECD copper is electrochemically deposited in the trench/via structures with a wide process window upon said seed layer and said barrier layer, with a fine grained <111> texture.

25. The method of claim 14, wherein each level of conducting structure is planarized by removing excess material, the method being selected from the group consisting of: planarization by chemical mechanical polish (CMP), milling, ion milling, and/or etching, which leave the copper in trench/via openings, forming single and dual inlaid structures that include conducting interconnect lines and contact vias.

26. The method of claim 14, wherein multilevel conducting structures are fabricating by repeating the process described herein.

27. A diffusion barrier structure formed in the fabrication of an integrated circuit comprising:

a semiconductor substrate;

a patterned insulating dielectric layer over said substrate, wherein the patterned insulating dielectric layer includes a dual inlaid opening trench/via structure, over an underlying interconnect;

a WN bottom or first diffusion barrier layer which is over said insulating dielectric layer and lines the trench/via structure;

a WSiN top or second diffusion barrier layer over said bottom WN layer;

a thin copper seed layer and thicker copper conducting layer are over the top barrier layer.

28. The structure of claim 27, wherein said barrier structure is formed in a trench/via cavity or opening and forms a trench/via liner, in small dimensional node applications of approximately 0.1 microns.

29. The structure of claim 27, wherein said barrier structure is formed with the first or bottom layer of WN, in the thickness range from about 60 to 400 Angstroms, and with the second or top layer of WSiN, in the thickness range from about 30 to 60 Angstroms.

30. The structure of claim 27, wherein said barrier structure in the trench or channel and the via hole contact is lined with an adhesive copper seed layer over the diffusion barrier layer, with seed layer thickness from about 200 to 2,200 Angstroms.

31. The structure of claim 27, wherein said barrier structure in the trench or channel and the via hole contact is covered with a conducting copper metal layer over the seed layer and diffusion barrier layer, forming conducting interconnect lines and contact vias, and is physically and electrically isolated by the barrier structure from undesirable regions.

32. A diffusion barrier structure formed in the fabrication of an integrated circuit comprising:

a semiconductor substrate;

a patterned insulating dielectric layer over said substrate, wherein the patterned insulating dielectric

layer includes a dual inlaid opening trench/via structure, over an underlying interconnect;

a WN bottom or first diffusion barrier layer which is over said insulating dielectric layer and lines the trench/via structure;

a WSiN second diffusion barrier layer over said bottom WN layer;

a W top or third diffusion barrier layer which is over said WSiN diffusion barrier layer;

a thin copper seed layer and thicker copper conducting layer are over the top barrier layer.

33. The structure of claim 32, wherein said barrier structure is formed in a trench/via cavity or opening and forms a trench/via liner, in small dimensional node applications of approximately 0.1 microns.

34. The structure of claim 32, wherein said barrier structure is formed with the first or bottom layer of WN, in the thickness range from about 60 to 400 Angstroms, and with an interposed or intervening layer of WSiN thickness from about 30 to 60 Angstroms, and top layer of W thickness from about 30 to 50 Angstroms.

35. The structure of claim 32, wherein said barrier structure in the trench or channel and the via hole contact is lined with an adhesive copper seed layer over the diffusion barrier layer, with seed layer thickness from about 200 to 2,200 Angstroms.

36. The structure of claim 32, wherein said barrier structure in the trench or channel and the via hole contact is covered with a conducting copper metal layer over the seed layer and diffusion barrier layer, forming conducting interconnect lines and contact vias, and is physically and electrically isolated by the barrier structure from undesirable regions.